Design and Optimization for Coaxial-to-Microstrip Transition on Multilayer Substrates

Hongwei Liang[1], Joy Laskar[1], Heidi Barnes[2], and Don Estreich[2]

[1]Packaging Research Center, School of Electrical and Computer Engineering,
Georgia Institute of Technology, Atlanta, GA 30332, Email: hwliang@ee.gatech.edu

[2]Microwave Technology Center, Agilent Technologies, Santa Rosa, CA 95403

***Abstract* — We present the design and optimization of a coaxial-to-microstrip transition on multilayer substrates for 10 GHz microwave applications. A parasitic parallel-plate line mode due to the multiple metal layers in the substrate has been observed from a careful electromagnetic field analysis. The parasitic mode causes serious leakage which can affect the embedded circuitry in the substrate significantly. A parasitic inductance has also been identified and suppressed. We apply an efficient comprehensive design method to develop a low-cost edge launch coaxial-to-microstrip interconnect on a six-metal-layer substrate. The new design shows no parasitic mode and no parasitic inductance. The final design demonstrates a return loss better than 20 dB at 10 GHz.**

I. INTRODUCTION

Multilayer printed wiring boards (PWBs) are very widely used in microwave and wireless industries. The input/output (I/O) of the radio frequency (RF) signal to the PWB is often realized using edge launch or right angle coaxial connectors. A soldering process is often used to attach the connectors to the PWB. The transmission line on the PWB is often designed in microstrip, thus the interconnection between the coaxial connector and the microstrip on the multilayer substrate is of great importance to the performance of a final module and system. It is not uncommon that to meet the strict electrical performance requirement at microwave frequencies, custom designed connectors and special assembly processes are required, adding cost to the final products [1]. To keep the cost of a microwave product as low as possible, it is highly desirable to use standard connectors and regular processes for the assembly of the connectors with the PWBs.

Although the coaxial-to-microstrip transition has a long history and broad range of application, there lacks careful examination from the aspect of electromagnetic (EM) analysis. Recent papers on coaxial-to-microstrip transition concentrates on modeling and characterization techniques [2]-[3]. Also, most of the research reported so far concentrates on the coaxial to a simple microstrip transition and does not cover the multilayer effect which can cause additional loss or coupling to the transition [1]-[4].

In this paper, we present a coaxial-to-microstrip transition on a six-metal-layer substrate using standard sub-miniature-A (SMA) coaxial connectors. The test structure, design method, and optimized design are presented in the following sections. We performed a full-wave analysis and found that there is a parallel-plate line (PPL) mode existing between certain grounding metal layers. We successfully eliminated the PPL mode in the new design. From a comprehensive measurement and analysis in both time and spectral domain, we also found and suppressed a parasitic inductance. The new design achieved a return loss better than 20 dB up to 10 GHz.

Fig. 1. A picture of the microstrip-to-coaxial transition on multilayer substrate. This test structure uses standard SMA connectors and a regular soldering process.

II. TRANSITION DESIGN

The coaxial-to-microstrip transition on a multilayer substrate is shown in Fig. 1. The microstrip line is on the top layer of a 6-metal-layer PWB, which is constructed with two different Rogers materials. The configuration of each layer in the PWB including the material property is shown in Fig. 2. The two layers constructed of the Rogers 4403 material are embedded between 3 thicker layers of the Rogers 4350 material to enhance the mechanical reliability of the board.

In the test structure, the microstrip signal line is constructed using a thick-film deposition process, and the substrate of the microstrip line occupies the first two layers of the PWB. The microstrip signal metalization is 35 mil wide and 1.5 mil thick, resulting in a 50 Ω characteristic impedance. The microstrip ground plane is on layer 3, and there is partial grounding metalization on

layer 1 to provide shielding to the signal line, as shown in Fig. 1. The layers 4, 5, and 6 were plated with metalization in the test structure. All grounding layers are electrically connected by several rows of vias, which provide the microstrip a good isolation from the adjacent circuitries. The SMA connector is finally attached to the board using a regular solder process.

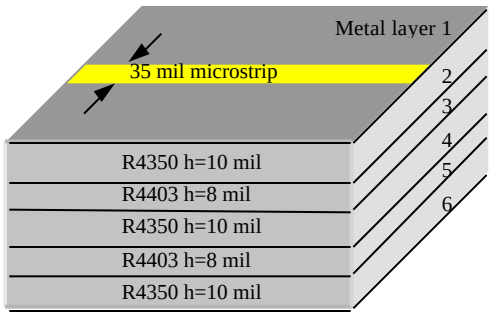

Fig. 2. The six-metal-layer substrate is constructed with two different materials: R4350 (ε_r=3.6, tan δ=0.004) and R4403 (ε_r=3.2, tan δ=0.005).

III. Analysis and Optimization

We applied a comprehensive analysis and optimization method as described in [5] to this structure. The method combines the ability of full wave analysis with the circuit analysis of the transition, and it has demonstrated a great efficiency in identifying the parasitics and generating solutions to remove them. It uses advanced microwave design tools [6]-[7] as design platforms and obtains both time and frequency domain response from a frequency domain simulation. The microwave design tool [6] is also used to perform the full-wave analysis. One of the advantages of this method is that it can identify independent sources of parasitics, such as parasitic inductance/capacitance or parasitic modes very quickly, and thus leads to new designs by optimizing the parameters, or eliminating the sources of parasitic modes.

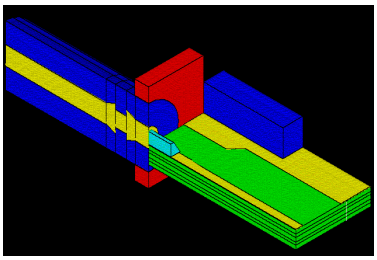

Fig. 3. 3-D model of the coaxial-to-microstrip transition on multilayer substrate for frequency domain simulation. Notice that the fine parts such as the barbs in the pin and the metal walls and fingers are included.

A 3-D model for the coaxial-to-microstrip transition was constructed for frequency domain simulation, as shown in Fig. 3. In order to achieve an accurate response from the model, detailed physical features of the transition are included, such as the barbs of the inner pin, the metal wall, and fingers of the SMA connector. The frequency domain response in S-parameters was obtained to 15 GHz. To get further insight, the S-parameter reflection data was converted to the time-domain using [7] to get the TDR response. Frequency- and time-domain measurements were also performed on the test structure using an HP8510 network analyzer. The measured and modeled data have a very good correlation, as shown in Fig. 4. The prototype shows a 15 dB return loss to 10 GHz.

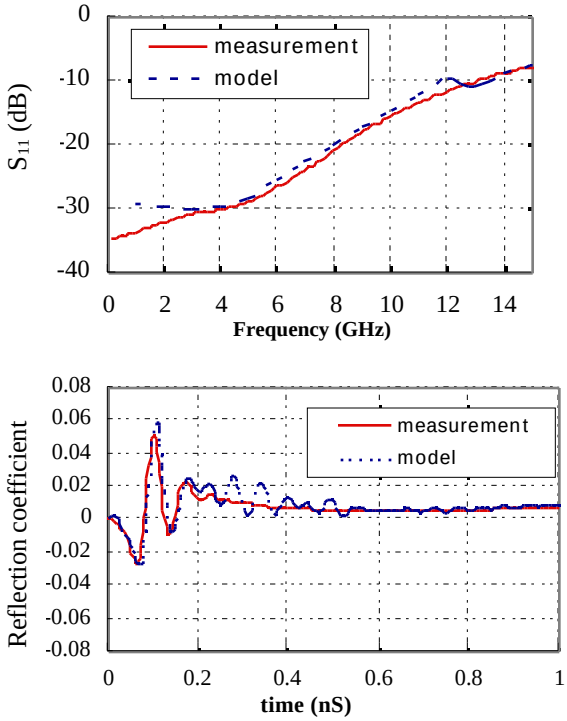

Fig. 4: Performance of the coaxial-to-microstrip transition on the multilayer substrate in frequency domain and time domain. The measurement and simulation matches very well.

A. Parasitic Mode

Using the comprehensive analysis method presented in [5], we discovered a PPL mode due to the multilayer substrate configuration. A TEM wave was excited at the port of the coaxial connector, as shown in Fig. 5(a). Near the interface to the microstrip line, the TEM wave mode is distorted and shows a non-cylindrical symmetry pattern, as shown in Fig. 5(b). The parasitic mode's field is strongest at the bottom half near the ground layers of the multilayer PWB. The field distribution at the cross-section of the PWB near the transition interface was

snapshot and shown in Fig. 6(a), where it can be clearly seen that the microstrip mode field is between layer 1 and 3, and the parasitic field is between all other grounding layers. The parasitic field appears to be stronger between layers 4 and 5 than other places. This is possibly because the smaller thickness between layer 4 and 5 is easier to support the PPL mode. Fig. 6(b) shows the field distribution pattern at a plane in the middle of layer 4 and 5.

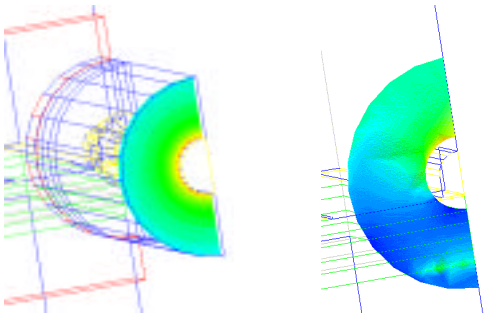

Fig. 5. E-field distribution patterns at two different cross sections of the coaxial connector. (a) TEM field pattern of the incident wave is shown at the port. (b) TEM mode is distorted and the parasitic mode has strong field at the bottom side of the cross section near the transition interface.

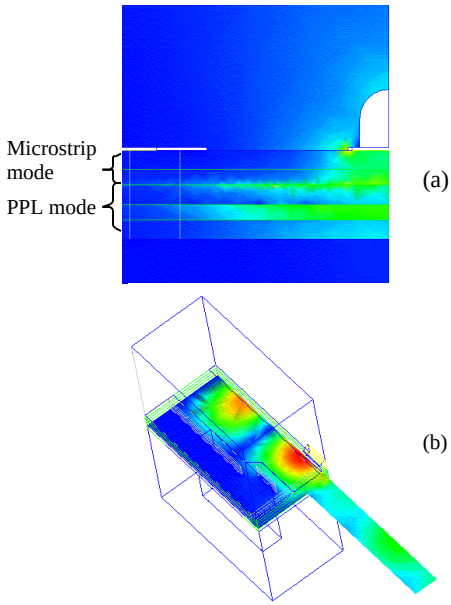

Fig. 6. Field distribution pattern in the multilayer substrate. (a) The microstrip mode is between layer 1 and 3, and the PPL mode is between each grounding layer from layer 3 to 6. (b) Field distribution across the middle plane of layer 4 and 5 shows a PPL mode.

In the new design, the parasitic mode is suppressed by shortening them to the ground. This can be achieved by a variety of methods. The one adopted in the new design is to use vias to connect the ground planes on all layers. A design with three added grounding vias at each side of microstrip line is shown in Fig. 7(a). The PPL mode is completely suppressed. It has been shown by the field at one vertical and one horizontal cross sections of the substrate, as in Fig. 7(b) and (c), respectively. The new design has a return loss better than 20 dB to 10 GHz.

The PPL mode may exist in other edge launch transitions such as coaxial-to-CPW [8] or coaxial-to-stripline structures when there are multiple metalization layers near the interface. It can cause undesirable coupling between electrically isolated components in the substrates and affect the performance significantly. In many cases, it can be suppressed by effectively shortening the adjacent grounding planes.

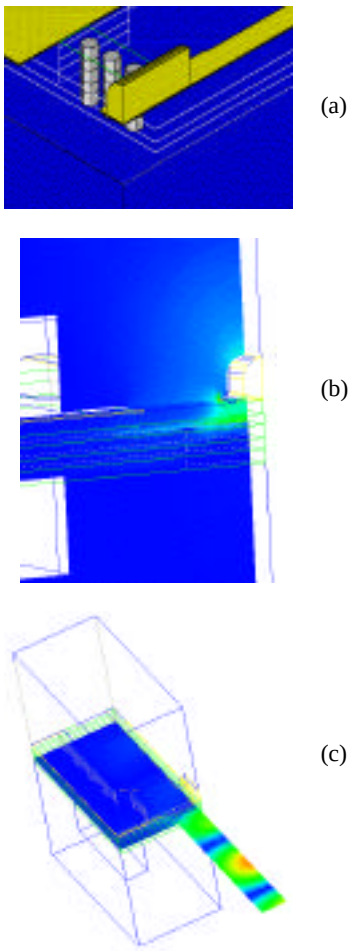

Fig. 7. New transition design with no PPL mode. (a) Three extra grounding vias are used to make the PPL mode shortened to the ground. (b) E-field distribution in the substrate at the cross-section near the interface (c) E-field distribution at a plane in the middle of layer 4 and 5. Both (b) and (c) show that the PPL mode is eliminated.

B. Parasitic Inductance

The comprehensive design method not only examines the structure from the EM field mode aspect, it also analyzes the structure in time-domain. The TDR response shows that the primary parasitics are inductive. The inductance is due to the high impedance region occurring at the ends of the microstrip line where the SMA pin is soldered to the board. To reduce the parasitic inductance, the microstrip line under the solder region is designed to be more capacitive to compensate the inductance. This is achieved by making the characteristic impedance lower by widening the microstrip line under the pin from 35 mils to 75 mils. The new design was simulated and it demonstrates a return loss better than 20 dB at 10 GHz, as shown in Fig. 8. The inductance associated with the transition is smaller than that in the old design. This is indicated in the TDR response of the two designs, as shown in Fig. 9.

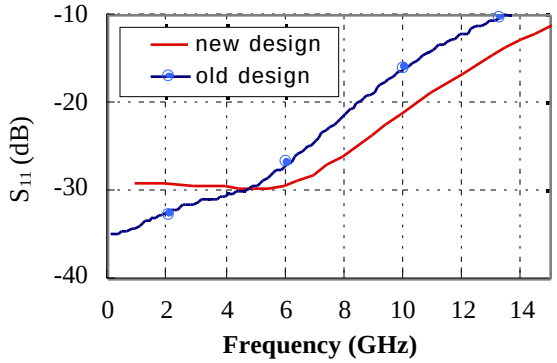

Fig. 8. Comparison of the return loss of the new and the old design.

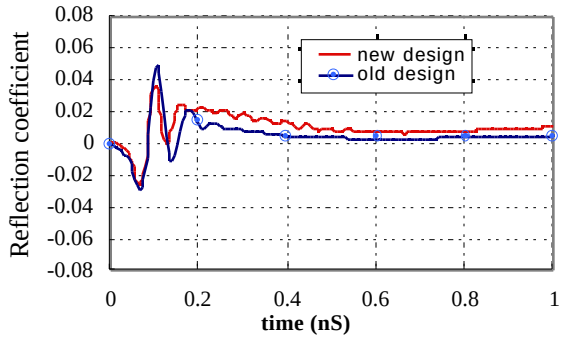

Fig. 9. Comparison of TDR response of the new and the old design.

IV. Conclusion

We report the analysis and elimination of a parasitic PPL mode in the coaxial-to-microstrip transition on a multilayer substrate. A parasitic inductance associated with the transition was also identified and suppressed. The comprehensive design method used in this paper demonstrated great efficiency in finding independent parasitic sources and improved design speed. The final design shows a better than 20 dB return loss and is suitable for 10 GHz applications. It is noteworthy that the PPL mode may exist in many other structures with edge launch transitions such as coaxial-to-CPW or coaxial-to-stripline when there are multiple metalization layers near the interface, and if not controlled properly, this can lead to unwanted coupling to the embedded circuitries in the substrates.

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